



## UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
 United States Patent and Trademark Office  
 Address: COMMISSIONER FOR PATENTS  
 P.O. Box 1450  
 Alexandria, Virginia 22313-1450  
[www.uspto.gov](http://www.uspto.gov)



CONFIRMATION NO. 1085

Bib Data Sheet

SERIAL NUMBER 10/774,588	FILING DATE 02/10/2004  RULE	CLASS 438	GROUP ART UNIT 2891	ATTORNEY DOCKET NO. 501.37465C10
-----------------------------	---------------------------------------	--------------	------------------------	-------------------------------------

## APPLICANTS

Yoshikazu Tanabe, Iruma-shi, JAPAN;

Satoshi Sakai, Tokyo, JAPAN;  
Nobuyoshi Natsuaki, Tokyo, JAPAN;

## \*\* CONTINUING DATA \*\*\*

This application is a CON of 10/424,105 04/28/2003 PAT 6,855,642  
 which is a CON of 09/939,600 08/28/2001 PAT 6,596,650  
 which is a CON of 09/494,036 01/31/2000 PAT 6,518,201  
 which is a CON of 09/380,646 09/07/1999 PAT 6,239,041  
 which is a 371 of PCT/JP98/00892 03/04/1998

## \*\* FOREIGN APPLICATIONS \*\*\*

JAPAN 9-50781 03/05/1997

## IF REQUIRED, FOREIGN FILING LICENSE GRANTED

\*\* 05/07/2004

Foreign Priority claimed	<input checked="" type="checkbox"/> yes <input type="checkbox"/> no	STATE OR COUNTRY	SHEETS	TOTAL	INDEPENDENT
35 USC 119 (a-d) conditions met	<input checked="" type="checkbox"/> yes <input type="checkbox"/> no <input type="checkbox"/> Met after allowance	JAPAN	DRAWING 21	CLAIMS 8	CLAIMS 1
Verified and Acknowledged	<i>V. Antonelli</i> <i>VY</i> Examiner's Signature Initials				

## ADDRESS

020457  
 ANTONELLI, TERRY, STOUT & KRAUS, LLP  
 1300 NORTH SEVENTEENTH STREET  
 SUITE 1800  
 ARLINGTON, VA  
 22209-3873

## TITLE

Method for fabricating semiconductor integrated circuit device

 All Fees